CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 6-9, 11 and 18-20 under 35 U.S.C. §112, second paragraph, and of claims 5, 11, 14 and 17 under 35 U.S.C. §112, first paragraph have been obviated by appropriate amendment and should be withdrawn.

The rejections directed to the claims that have not been amended are respectfully traversed. For example, the rejection of claims 7 is not proper and/or understandable. Applicant's representative respectfully requests that the Examiner either (i) withdraw such rejections or (ii) provide detailed statutory authority for the rejections.

CLAIM REJECTIONS UNDER 35 U.S.C. §102(b)

The rejection of presently pending claims 1-4, 6, 12-13 and 15-16 as being anticipated in view of Davis et al. '271 is respectfully traversed and should be withdrawn.

Davis et al. disclose a synthesized clock microcomputer with power saving (title). Davis et al. is silent with regard to a programmable logic circuit, as in presently pending claims 12, 15 and 22. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, Davis et al. is silent with regard to a product term array and a look-up table, as in presently pending

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claims 3 and 4. As such, claims 3 and 4 are independently patentable over Davis et al.

CLAIM REJECTIONS UNDER 35 U.S.C. §102(e)

The rejection of presently pending claims 1-2, 4, 6-9 and 12-13 as being anticipated in view of Weiss et al. '703 is respectfully traversed and should be withdrawn.

Weiss et al. disclose a data processing system having a register controllable speed. FIG. 4 of Weiss et al. shows a clock input divided into a number of clocks by the dividers block 404. Weiss et al. do not disclose or suggest a programmable logic circuit and a phase lock loop circuit, integrated on a single circuit, as presently claimed. As such, presently claim invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 5, 7, 10-11, 14 and 17-20 as being obvious over Davis et al. in view of Hotta et al. is respectfully traversed and should be withdrawn. Hotta et al. fail to teach or suggest providing a plurality of internal clock signals each capable of operating at a different one of a plurality of frequencies in a programmable logic circuit, as in presently pending claims 12, 15 and 22. Furthermore, Davis et al. is silent

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with regard to programmable logic devices. It follows that Davis et al. cannot cure the deficiencies of Hotta et al., with respect to programmable logic devices. Hence, neither of the references, alone or in combination, teach or suggest a programmable logic circuit and a phase lock loop circuit integrated on a single circuit, as presently claimed. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

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If any additional fees are due, please charge our office Account No. 02-2712.

Respectfully submitted,

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